REMARKS

Upon entry of the present amendment, claim 3 will be canceled without prejudice or disclaimer of the subject matter recited therein, and claim 1 will be amended, whereby claims 1, 2 and 4 will remain pending with claim 1 being the sole independent claim.

While not expressing agreement or acquiescence with the rejections of record, claim 1 has been amended to even more explicitly recite the via holes including that the "the via holes are filled with solder or electric conductive paste". Support for the amendment to claim 1 appears in Applicants' originally filed application, including the paragraph beginning the bottom of page 24 through the first full paragraph on page 25. Accordingly, no new mater should be considered to be introduced by the present amendment.

Reconsideration of the rejections of record and allowance of the application in view of the following remarks are respectfully requested.

Discussion of Child Application

Applicants note that a divisional application has been filed of the present application and has been awarded Application No. 12/410,069, published as US 2009-0186431 A1. A Quayle Office Action has been mailed in the divisional application. The Examiner is requested to review the file history of the divisional application at the Patent and Trademark Office, which is being examined by the same Examiner as the present application.

Moreover, the following documents have been cited in the Quayle Office Action:

U.S. Patent No. 6,316,785 to Nunoue et al.

U.S. Patent No. 5,693,963 to Fujimoto et al.

Applicants are submitting herewith a Form 1449 as an Information Disclosure Statement listing the above-noted documents, and the Examiner is requested to indicate consideration of these documents by including an initialed copy of the form with the next communication from the Patent and Trademark Office. Copies of the documents are not submitted herewith as the documents are a U.S. patent application, a U.S. patent application publication or U.S. patents for which copies need not be provided

A fee should not be necessary for consideration of this Information Disclosure Statement. However, authorization is hereby provided to charge any necessary fee for consideration of the information provided to Deposit Account No. 19-0089.

Response To Rejections

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 6,333,522 to Inoue et al. (hereinafter "Inoue") in view of U.S. Patent Publication No. 2004/0026708 A1 to Chen and further in view of U.S. Patent Publication No. 2003/0160258 to Oohata.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue and Chen and Oohata, and further in view of U.S. Patent No. 6,878,973 to Lowery et al. (hereinafter "Lowery").

In response to these grounds of rejection, Applicants submit that none of the documents of record teaches or suggests, as recited in Applicants' independent claim 1 a light-emitting device formed by depositing p-type and n-type nitride semiconductor layers, comprising:

deposited p-type and n-type nitride semiconductor layers;

semiconductor-surface-electrodes to apply currents into each of the semiconductor layers;

an insulating layer which holds the semiconductor layers, said insulating layer comprising two surfaces; and

mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder, the mount-surface-electrodes being provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made;

wherein one of the semiconductor layers has a non-deposited area where the other semiconductor layer is not deposited;

one of the semiconductor-surface-electrodes is built up on the surface of the non-deposited area;

via holes are made in the insulating layer which electrically connect the semiconductor-surface-electrodes and the mount-surface-electrodes, the via holes are filled with solder or electric conductive paste;

the semiconductor-surface-electrodes, the insulating layer, and the mount-surface-electrodes are built up in this order on one side of the deposited semiconductor layers; and

a surface of the other side of the deposited semiconductor layers is a light emitting surface which emits light beams directly to outside from the semiconductor layers.

Applicants submit that any combination of the prior art, even if the prior art is properly combinable, does not teach or suggest Applicants' recited subject matter which includes, amongst other features set forth in the recited combinations, via holes are made in the insulating layer which electrically connect the semiconductor-surface-electrodes and the mount-surface-electrodes, the via holes are filled with solder or electric conductive paste. In this regard, the

Examiner's attention is directed to Applicants' specification in the paragraph beginning at the bottom of page 24 and continuing through the first full paragraph on page 25.

Additionally, the Examiner's attention is directed to Applicants' specification at page 5, lines 9-15, wherein it is disclosed that:

> By such a configuration, since electric conductor is generally good thermal conductor, the heat generated at semiconductor layers, which constitute light-emitting portion, can be efficiently radiated through the electric conductor filled in the VIA's to the board on which the device is mounted, and it is possible to lower the thermal load to the light-emitting device, and is possible to realize stable light extraction and long life-time of the light-emitting device.

Moreover, it is disclosed at the paragraph appearing at beginning at the bottom of page 24 through the top of page 25 that:

> The improvement of the heat radiation performance by VIA is described. FIG. 9 shows filled VIA's. When the electrical conductor 51 in the VIA holes 41 is formed, by filling up the VIA holes with electrical conductor 51, which is also good thermal, a filled up VIA structure can be made, and with this structure it is possible to improve the heat radiation of the semiconductor layers 2,3, that is, light-emitting portion. The filling with the electric conductor can be done by thick plating to the inner surface of the VIA holes 41. Alternatively, the VIA holes 41 may be filled with electric conductive paste. Material of high thermal conductivity is preferable as the filling material. For example, copper (403W/m/K), silver (428W/m/K), aluminum (236W/m/K) are such material. Furthermore, the larger the planar dimension of VIA hole is the better for improvement of heat radiation. The improvement of heat radiation results suppression of thermal load for light-emitting device, and stable light extraction can be achieved.

Moreover, it is disclosed at the paragraph appearing at page 25, first full paragraph, of Applicants' specification, that:

> As another filling method for VIA holes 41, as shown FIG. 10A and FIG. 10B, a method using solder is available, where the solder is used for mounting the device onto mounting substrate 54. The thermal conductivity of the solder is, for example, 50 W/m/K, and solder can efficiently dissipate the heat. For the mounting of the light-emitting device, the device mounting process in the print-circuit board technologies can be used, and therefore no special mounting process is necessary, and the mounting process can be made simple too.

In contrast to Applicants' recited subject matter, Inoue which is used in the rejection in an attempt to try and establish the obviousness of Applicants' claim 3, does not teach or suggest "via holes filled with solder or electric conductive paste". Inoue discloses, for example, at column 21, lines 23-34 page, the forming of microbumps by selectively plating with Au. Moreover, Inoue discloses at column 26, beginning at line 52 that, "The material of the microbumps may be solder material or Au-based material." Thereafter, still referencing microbumps, Inoue discloses the benefits and disadvantages of solder and Au-based material as well as advantages and disadvantages of the stud bump and plating methods.

Accordingly, Inoue et al. discloses microbumps made of solder or gold, but does not disclose "via holes filled with solder or electric conductive paste". In contrast, microbumps as disclosed by Inoue are projected electrodes used to mount a chip on a substrate as compared to via material used to electrically and thermally connect semiconductor-surface-electrodes with mount-surface-electrodes, and not used for mounting.

Moreover, as previously noted by Applicants, in contrast to the subject matter recited in Applicants' independent claim 1, and further defined in the dependent claims, Inoue does not teach or suggest a light-emitting device including, amongst the combination of features, mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder. The light-emitting device disclosed by Inoue is structured and arranged for microbump mounting, as see, for example, the Abstract of Inoue. In contrast to the subject matter recited in Applicants' independent claim 1, and further defined in the dependent claims, Inoue does not teach or suggest a light-emitting device including, amongst the combination of features, mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder. The light-emitting device

disclosed by Inoue is structured and arranged for microbump mounting, as see, for example, the Abstract of Inoue.

Therefore, for at least the reasons set forth above, the rejections of record should be withdrawn.

Moreover, Applicants note that the use of solder or electric conductive paste allows for desired heat dissipation effect being obtained at lower cost and more easily than by using gold electro-plating. For gold electro-plating, there is needed a tie-bar for plating-current as well as the removal of the tie-bar in a post-process. For electroless plating, control or management of solution is complex, and plating speed is low and inefficient. For both plating methods, large facilities such as control systems for solution control and plating baths are necessary. Moreover, the plating material is gold and gold is expensive.

In contrast, for solder or electric conductive paste, the material can be mechanically filled, and no additional configuration for via such as tie-bar for plating current is necessary. Filling speed is higher than with plating. Filling can be done by using a compact tool such as a dispenser or a screen printing machine. The process does not require liquid, and therefore control systems for solution control and plating baths are not necessary. The filling material is cheaper than gold. Therefore, the via can be enlarged to fill large amount of filling material, and good heat dissipation efficiency equivalent or prevail to the heat transfer by gold plating is performed. Moreover, the light-emitting device of this invention can be a device that can be mounted by surface-mount-technology, and such device can be provided with larger size vias than the device mounted without using surface-mount-technology.

Accordingly, for at least the reasons set forth above, each of the rejections of record should be withdrawn, and the application should be allowed

CONCLUSION

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections of record, and allow each of the pending claims.

Applicants therefore respectfully request that an early indication of allowance of the application be indicated by the mailing of the Notices of Allowance and Allowability.

Should the Examiner have any questions regarding this application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
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